

REMARKS

Status of Claims:

Claims 1-15 are present for examination.

Drawing Correction:

Applicant's submit herewith a replacement sheet for Figure 14 in which Fig. 14 is labeled as "Prior Art" as requested by the examiner.

Rejections under § 112:

Claims 9-11 stand rejected under 35 U.S.C. §112, ¶2 as being indefinite. Applicant has amended the claims to remove the grounds for the 112 rejection. It is submitted that all of applicant's claims now fully comply with the requirements of Sec. 112.

Prior Art Rejection:

Claims 1-3 and 7-11 stand rejected under 35 U.S.C. §103 as unpatentable over Goto. Further, claims 4, 6 and 12-15 stand rejected under 35 U.S.C. §103 as unpatentable over Goto in view of AAPA.

The examiner's rejections are respectfully traversed.

The present invention relates to a clock generating circuit which can compensate the clock skew caused by manufacturing variations in the semiconductor integrated circuit device and the duty ratio, and in addition minimize jitter by using the delay adjustment circuit having a delay time interval which can be regulated by controlling the internal register values and the internal signals of the semiconductor integrated device and external signals (see page 3, lines 9 to 14 in the originally filed specification of the present patent application).

In contrast, the Goto teaches a document which discloses an inspecting apparatus for mixed signals in an LSI such as CMOS. Goto does not disclose nor indicate that the inspection apparatus may be used for an LSI such as a CMOS; therefore, there is not any

motivation for one of skill in the art to make use of the content of the Goto so as to realize the present invention.

In particular, the Examiner commented that the FE element in FIG. 4b of Goto correspond to a first gate array. However, FIG. 4 of Goto is a graph which does not indicate the "FE." Thus, it is believed that the Examiner's rejection is inconsistent with the drawing.

Applicant understands that it is feasible that FIG. 4b may be a typological error and that the Examiner may have intended to refer to FIG. 6 of Goto. However, even in this figure, a control device which controls a first switching device and a second switching device so as to adjust the delay time internal of the input signal is not disclosed nor indicated in the Goto.

Conclusion:

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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